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CS 5780

Lab 2 Pre-Lab

1. What is the purpose of the NVIC peripheral? (section 3.3.1)

The NVIC peripheral enables and disables interrupts, indicate requests waiting to be serviced, cancels pending interrupt requests, and sets how multiple interrupts interact using configurable priorities.

1. What is the difference between interrupt tail-chaining and nesting? (section 3.3.2)

In tail chaining when multiple interrupt triggers happen concurrently or during a handler, they are executed one after each other according to the hardware priority. Or in other words interrupt handlers are never interrupted. In nesting the NVIC allows important interrupts to interrupt lower priority handlers. It requires a more complex context-switch mechanism but otherwise works how interrupts normally pause execution of the main application thread.

1. In what file are the CMSIS libraries that control the NVIC? (section 3.3.4)

They are in the core\_cm0.h file.

1. What is the purpose of the EXTI peripheral? (section 3.4.1)

It is a peripheral that allows non-peripheral sources to trigger interrupts.

1. What is the purpose of the SYSCFG pin multiplexers? (section 3.4.1)

The multiplexers main purpose is to group external pins by their orderings within the GPIO peripherals. It is up to the SYSCFG to deal with signal routing and controls data transfer between peripherals and memory, remapping portions of memory, and some high-power communication modes.

1. What file has the defined names for interrupt numbers? (section 3.5.1)

They are located in the stm32f072xb.h file.

1. What file has the Vector table implementation? (section 3.2 or 3.5.2)

The Vector Table implementation is located in the startup\_stm32f072xb.s file.